IN THE CLAIMS

The pending claims are reprinted below:

1. (Original) A computerized method for identifying structural regularity in a logic design, the method comprising:

receiving a plurality of templates covering the logic design;

receiving one or more control signals for the logic design;

receiving one or more databus identifiers for the logic design; and

generating a first vector for the logic design through computer automated operations to combine at least one instance of one of the plurality of templates based on the control signals, the databus identifiers and connectivity of the logic design.

2. (Original) The computerized method of claim 1 wherein the first vector comprises each one of the instances of a first one of the templates having a same set of the control signals and feeding a same databus.

3. (Original) The computerized method of claim 2 wherein a second vector is generated from each one of the instances of a second one of the templates having a same set of connections in the logic design.

4. (Original) The computerized method of claim 1 wherein the plurality of templates is received in a net list.

5. (Original) The computerized method of claim 1 wherein at least one of the plurality of templates is a tree template.

6. (Original) The computerized method of claim 1 wherein at least one of the plurality of templates is a multi-output template.

7. (Original) The computerized method of claim 1 wherein at least one of the plurality of templates is a single-principal output template.

8. (Original) A computerized method for generating a set of vectors for a logic design through computer-automated operations, the method comprising:

identifying logic for generating at least one control signal and excluding the logic from the set of vectors;

identifying at least one instance of a first template to group as a first vector in the set of vectors by using databus identifiers and the control signals; and

identifying at least one instance of a second template to group as a second vector in the set of vectors by using circuit connectivity and a previously formed vector.

9. (Original) The computerized method of claim 8, wherein identifying at least one instance of the second template using circuit connectivity and a previously formed vector is performed after all possible vectors are identified using the databus identifiers and the control signals.

10. (Original) The computerized method of claim 8 wherein the logic design is for a datapath circuit.

11. (Original) A computerized method of generating a layout for a logic design using vectors, the method comprising:

receiving one or more vectors for the logic design;

receiving connectivity data for the logic design; and

generating a one-dimensional circuit layout for the logic design through computer automated operations using the vectors and the connectivity data.

12. (Original) The computerized method of claim 11 wherein generating the one-dimensional layout further comprises:

enumerating a plurality of solutions for the layout;

calculating a total wire length for each one of the solutions; and

selecting the solution with a minimum wire length.

13. (Original) The computerized method of claim 11 further comprising receiving critical path data for the logic design.

14. (Original) The computerized method of claim 13 wherein generating the one-dimensional layout further comprises:

enumerating a plurality of solutions for the layout;

calculating a cost for each one of the solutions; and

selecting the solution with a minimum cost for the critical path.

15. (Original) The computerized method of claim 11 wherein each one of the vectors forms a row in the one-dimensional circuit layout.

16. (Original) The computerized method of claim 11 wherein the logic design is for a datapath circuit.

17. (Original) A machine-readable media having machine-executable components comprising:

a functional regularity extraction component to generate a plurality of templates to cover a logic design;

a structural regularity extraction component to generate a set of vectors from the plurality of templates; and

a floorplanning component to generate a circuit layout from the set of vectors.

18. (Original) The machine-readable media of claim 17, wherein a vector in the set of vectors is a group of template instances that are identical in function and structure.

19. (Original) The machine-readable media of claim 17 wherein the structural regularity

extraction component further comprises:

a control logic identifying component to identify logic for generating at least one control signal and excluding the logic from the set of vectors;

a first vector identifying component to identify at least one instance of a first template to group as a first vector in the set of vectors by using databus identifiers and the control signals; and

a second vector identifying component to identify at least one instance of a second template to group as a second vector in the set of vectors by using circuit connectivity and a previously formed vector.

20. (Original) An article comprising:

a machine-readable media including instructions that when executed cause a computer to:

receive a plurality of templates covering the logic design;

receive one or more control signals for the logic design;

receive one or more databus identifiers for the logic design; and

generate a first vector for the logic design through computer automated operations to combine at least one of the plurality of templates based on the control signals, the databus identifiers and connectivity of the logic design.

21. (Original) The article of claim 20 wherein the first vector comprises each one of the instances of a first one of the templates having a same set of control signals and feeding a same databus.

22. (Original) The article of claim 21 wherein a second vector is generated from each one of the instances of a second one of the templates having a same set of connections in the logic design.

23. (Original) An article comprising:

a machine-readable media including instructions that when executed cause a

computer to:

identify logic for generating at least one control signal and excluding the logic from the set of vectors;

identifying at least one instance of a first template to group as a first vector in the set of vectors by using databus identifiers and the control signals; and

identifying at least one instance of a second template to group as a second vector in the set of vectors by using circuit connectivity and a previously formed vector.

24. (Original) The article of claim 23, wherein identifying at least one instance of a second template using circuit connectivity and a previously formed vector is performed after all vectors are identified using the databus identifiers and the control signals.

25. (Original) An article comprising:

a machine-readable media including structural regularity extraction instructions that when executed cause a computer to generate a set of vectors from a plurality of templates.

26. (Original) An article comprising:

a machine-readable media including floorplanning instructions that when executed cause a computer to generate a circuit layout from a set of vectors.